FPGA Implementation of Digital Transmitter for Software Defined Radio

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Abstract

In this paper, we present the architecture and implementation of an all-digital transmitter with radio frequency output targeting an FPGA device. FPGA devices have been widely adopted in the applications of digital signal processing (DSP) and digital communication. They are typically well suited for the evolving technology of software defined radios (SDR) due to their reconfigurability and programmability. However, FPGA devices are mostly used to implement digital baseband and intermediate frequency (IF) functionalities. Therefore, significant analog and RF components are still needed to fulfill the radio communication requirements. The all-digital transmitter presented in this paper directly synthesizes RF signal in the digital domain, therefore eliminates the need for most of the analog and RF components. The all-digital transmitter consists of one QAM modulator and one RF pulse width modulator. Our work extends the digital implementation of communication applications on an FPGA platform to radio frequency, therefore making a significant evolution towards an ideal SDR.

Keywords: Software Defined Radio (SDR), OFDM Modulator, Sample Rate converter

I. Introduction

There are many kinds of wireless communication systems currently in use. Software defined radio (SDR) technology is needed for multimode and multi-standard communication devices, allowing end users to move between domains and footprints and maintain serviceability [2, 11]. One definition of SDR is: an SDR is a radio in which the digitization is performed at some stage downstream from the antenna. Then the radio can use flexible and reconfigurable hardware such as FPGAs to implement the digital signal processing algorithms. As technology advances, for an ideal SDR, the digitization might be at, or very close to the antenna, such that almost all the radio communication functionalities can be realized using software based on high speed and reprogrammable digital signal processing engine [14]. However, current SDR implementations still require significant amount of analog components. An example of a current SDR based transmitter architecture [3] is shown in Figure 1. In this paper, we try to tackle this problem and show the feasibility of an all-digital transmitter illustrated in Figure 2. Almost all the transmitter’s functionalities can be incorporated in the digital signal processing engine using FPGAs except the RF power amplification and simple filtering. The advantages of all-digital transmitters are: potential high efficiency power amplification ([810]), the capabilities of digitally combining signals from multiple channels, and software programmability.

Figure 1. Current SDR based transmitter architecture
presented in literature [8, 10, 16]. In these works, the digital RF signals were computed offline and stored in pattern generator for the purpose of measurement. In this paper, we present the architecture and implementation of a real-time system that demonstrates the feasibility of digital generation of RF signals.

In this section, we present the architecture and the FPGA implementation of our universal QAM modulator. The all-digital transmitter consists of two major functional blocks: a universal QAM modulator and a radio frequency pulse width modulator (RFPWM). The entire transmitter is implemented on a Xilinx’s Virtex2pro device. The binary output of the transmitter is centered at 800 MHz with 64QAM signaling format. Figure 3 shows the overall architecture of our all-digital transmitter.

traditional modulator, a quadrature direct digital frequency synthesizer (QDDFS) will be used to modulate the signal to intermediate frequency (IF), and then the digital output is converted to analog signal using DAC [1, 15]. In the all-digital transmitter presented in this paper, an RFPWM will be used to directly synthesize RF signals in digital domain.

The QAM modulator consists of several digital interpolation filters. The pulse shaping filter is used in almost all digital modulators to minimize inter-symbol interference (ISI). The pulse shaping filter is made programmable such that it is flexible to accommodate different standards and modulation formats. The three half-band filters further increase the sampling rate, which can reduce the complexity of the sample rate converter. The combination of pulse shaping filter and the subsequent halfband interpolation filters are sometimes referred to as multi-stage upsampling filters. The pulse shaping filter and half band filters all have integer interpolation ratios, therefore the sampling rate of the last half-band filter’s output is an integer multiple of the input symbol rate. A sample rate converter is generally needed to convert this sample rate to another arbitrary

2. UNIVERSAL QAM MODULATOR

In this section, we present the architecture and the FPGA implementation of our universal QAM modulator. The overall QAM modulator architecture is presented in Section 2.1. In Section 2.2, we present the details of the main functional blocks inside the modulator and their implementations.

2.1 Universal QAM Modulator Architecture

Figure 4 shows the block diagram of the QAM modulator. The double lines connecting different blocks indicate that there are two identical datapaths for both inphase path and quadrature path (I and Q). In a
sample rate. The reason for this conversion is that SDR based transmitter is required to support multiple air-interface, where each air-interface often specifies its unique symbol rate. In order to allow the digital to analog converter to have a constant sample rate regardless of the input symbol rate, a sample rate converter is needed. Although no DAC is needed in our all-digital transmitter, a sample rate converter (SRC) is still necessary to convert the sample rate to a fixed sample rate suitable for PWM generation.

2.2 FPGA Implementation of the Modulator

2.2.1 Multi-stage Upsampling Filters

The multi-stage upsampling filters consist of one pulse shaping filter and three stages of halfband interpolation filter. The pulse shaping filter is the most complex filtering operation in the QAM modulator. Finite impulse response (FIR) filters are normally used for pulse shaping due to their linear phase responses. The impulse response of a linear phase FIR is either symmetrical or anti-symmetrical. Design techniques of FIR filters have been well studied for ASIC implementations [7]. In this paper, we present the general interpolation FIR architecture specifically optimized for FPGAs.

There is an inherent interpolation operation in the pulse shaping filter. Interpolation filters can be efficiently implemented using polyphase structures by dividing the original filter into subfilters [7]. Efficient FIR implementations take advantage of the filter coefficients symmetry to minimize the number of multiplications. It has been shown that when the interpolation ratio is even and the length of the FIR filter is odd, we can have two linear phase subfilters after decomposing into polyphase structure [7]. Therefore we choose the interpolation ratios to be two for all of the interpolation filters, while designing them to have odd number of taps.

Our FIR architecture is shown in Figure 5. It consists of two linear phase FIR engines for the two subfilters respectively. Inside each FIR engine, the datapath takes advantage of the coefficients symmetry in the filter by performing the summation of two input samples before the multiply and accumulate (MAC) takes place. The additional input to the accumulator adder (acc_in) is needed when the input sample rate is too high for one FIR engine to complete all the calculation before the next input sample arrives. In that case we need to daisy chain several FIR engines together to pipeline the operation. The FIR output from one stage of the pipeline will be connected to the acc_in input of the next stage. We implemented both the input buffer and coefficient RAM using the distributed memory in Xilinx FPGA. Although the two subfilters are working on the same set of input, they require different ordering of the samples. Therefore a re-ordering block is designed to temporarily store the samples read from the buffer and then present them to the FIR engines at the appropriate time.

The halfband filter is a special class of FIR filter. Every other coefficient of the halfband filter is zero. Therefore by combining this special property together with the general coefficient symmetry of the linear phase FIR filter, the implementation of halfband filter can be very hardware efficient. In addition, the halfband filters in a digital modulator often have fixed coefficients. These coefficients can be formatted using canonic signed digits (CSD) [7]. By using CSD formatted coefficients, the multiplication and accumulation in a general FIR can be replaced by shift and add operation instead.

![Figure 5. Interpolation FIR implementation architecture](image)

2.2.2 Sample Rate Converter

As shown in Figure 4, sample rate converter (SRC) is needed to convert the digital signal from one sampling to another sampling rate while preserving the necessary information [4]. The underlying operation of an SRC is interpolation, where new sample values at arbitrary time instants in
between the existing samples are computed. The sampling time offsets between the new sampling instants and original sampling instants are referred to as fractional intervals $\mu_k$. The SRC can be possibly implemented using traditional FIR architecture, where the coefficients for this FIR filter vary with the fractional interval $\mu_k$. Then pre-computed coefficients need to be stored in memory for each possible $\mu_k$. When the number of elements in the set of $\{\mu_k\}$ becomes very large to achieve fine resolution on fractional interval, the memory requirement to store the coefficients can be high. Instead, in this paper, we use polynomial based interpolation, which does not require any storage of filter coefficients. In contrast, the coefficients can be computed based on the fractional interval value $\mu_k$. Moreover, a hardware efficient architecture, Farrow structure, can only be applied to polynomial based SRC. The details about Farrow structure can be found in [4].

The architecture of the sample rate converter is shown in Figure 6. The SRC consists of: 1) the numerically controlled oscillator (NCO) that supplies the fractional interval $\mu_k$ and manages the input buffer of SRC; 2) the Farrow computation structure that calculates the SRC output. The NCO is programmed by a frequency control word (FCW), determined by the ratio of the input sample rate and output sample rate ($F_{in}/F_{out}$). Different symbol rates can be supported by reprogramming the FCW. We assume the ratio is less than 1, therefore interpolation (sample rate increase) rather than decimation (sample rate decrease) is always performed.

![Figure 6. Complete sample rate converter architecture](image)

**Figure 6. Complete sample rate converter architecture**

Through the NCO, the SRC is able to maintain the input rate at $F_{in}$ while generating output at the rate of $F_{out}$. One important signal from the NCO is the accumulator overflow signal, which asserts at the rate of $F_{in}$. Whenever the NCO overflows, a new input sample is needed to calculate SRC output. We introduce a buffer between the output of the multi-stage upsamplers and the sample rate converter. Every time the NCO overflows, the buffer pointer will be incremented and a new sample is read from the buffer. The same signal is also used to enable the new sample to be shifted into the delay line. Also, the NCO register value represents the fractional interval. Only a number of MSBs from the register are needed for the SRC computation to meet our performance requirement, such as ACLR and EVM.

Moreover, the NCO overflow indicator is divided by $M$ in frequency to generate a “request for data” (RFD) signal to the multi-stage upsampling filters, where $M$ is the aggregate interpolation ratio of all the filters consisting of the multistage upsampling filters. For example, in our QAM modulator architecture shown in Figure 4, the value of $M$ should be set to 16. Upon receiving the RFD signal, the multi-stage upsampler reads one symbol through the input interface, and will produce $M$ output samples to the SRC input buffer after performing the interpolations. Using this mechanism, the SRC buffer is guaranteed to maintain its fill level around some balanced state without experiencing any overflow or underflow.

A different control approach is to use the MSB of the NCO register as the reference clock for the delay line as shown in Figure 6. This reference clock is further divided down to provide sample rate clocks to the different interpolation filters inside the multi-stage upsampling filters [1, 15]. The novelty of our implementation only requires one system clock for all the filter stages. The rate control is accomplished by the request-and-respond between SRC and multi-stage upsamplers. By using such a handshake interface mechanism, it is possible to implement the multi-stage upsampling in an independent platform such as a digital signal processor.

### 3. Implementation Results

The entire all-digital transmitter architecture is shown in Figure 11. Only the functional blocks for inphase path are shown in detail, while the quadrature path consists of almost identical functional blocks. In order to accommodate the parallel transformation of the PWM signal processing, the sample rate converter is modified to a parallel architecture.

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4. RELATED WORK

The related work presented in the literature can be grouped into two categories. The first category consists of architectural study and implementation of digital modulators and transmitters. All digital modulators implemented on ASIC were presented by Cho and Samueli [1] and Vankka et al. [15]. SDR based architecture using FPGAs is presented by Lee et al. [9] and Sheen et al. [13] for CDMA2000 and WCDMA, respectively. All of these transmitters are based on digital IF architecture, therefore require highly sensitive analog and RF components such as wideband DAC. The all-digital transmitter architecture presented in this paper eliminates the IF stage by directly synthesizing RF signal in digital domain. The other category consists of algorithm study or partial implementation of digital RF generation. Keyzer et al. [8] describe a digital transmitter using BPDS architecture. The high rate of processing makes it very difficult for implementation. RFPWM algorithm and simulation results were presented in Midya et al. [11]. Wagh et al. [16] present a digital RF transmitter based on digital PWM, however the duty ratios were computed offline and then fed to the PWM generator for testing. This paper presents the implementation of a complete all-digital transmitter with RF output.

5. CONCLUSION

Software defined radio (SDR) technology enables wireless infrastructures and devices to support multiple air-interfaces, by using reconfigurable hardware platform. From the transmitter point of view, the current SDR architecture still contains highly sensitive analog and RF components which are hardly software definable. In this paper, we extend the software defined functionalities to radio frequency with the novel all-digital transmitter. The all-digital transmitter uses pulse width modulation (PWM) method such that the RF signal with binary format can be directly synthesized in digital domain. The low rate of the signal processing of PWM makes it suitable for implementation on off-the-shelf FPGA devices. By combining a universal QAM modulator and an RF pulse width modulator, we demonstrated a real time transmitter system with digital RF output using realistic signaling format, i.e., 64QAM. The on chip multi-gigabit transceiver (MGT) is used to generate 3.2Gbps binary RF signals, with 800 MHz carrier frequency. The measured passband ACLR is about 45 dB. The measured EVM is less than 1%. With the advancement of FPGA technology, the all-digital transmitter presented in this paper will help to make a feasible ideal SDR in the future.

6. REFERENCES


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