Design of Power-Efficient Digital Circuits Using Gate-Diffusion Input (GDI) Technique in CMOS Process

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Abstract—In this paper, Gate diffusion input (GDI) technique of Low-power digital circuit design is described and verified in 0.18µm CMOS process. This technique permits reducing power consumption, propagation delay, and area of digital circuits of logic design. Performance comparison with traditional CMOS and pass-transistor logic design techniques is presented. These methods are compared with respect to the layout area, number of devices and power dissipation. Basic logic Gates have been implemented in various design styles. Their properties are discussed, simulation results are reported.

Index Terms—Analysis, CMOS, digital, low-power design, performance, VLSI.

I. INTRODUCTION

The rapid development of portable digital applications in VLSI, the demand for increasing speed, compact implementation, and low power dissipation activates numerous research efforts [1]–[3]. The demand to improve the performance of low power VLSI applications, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last decades. One form of logic that is popular in low-power digital circuits is CMOS logic. In this paper offers a new low-power design technique that allows solving most of the problems like low power and transistor count. The GDI method allows implementation of a wide range of complex logic design functions using only two transistors. GDI technique is suitable for design of fast, low-power circuits, using a reduced number of transistors as compared to CMOS logic design technique.
III. IMPLEMENTATION OF BASIC FUNCTION USING GDI LOGIC

Table I shows simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Best of these functions are complex required 6–12 transistors in CMOS logic, as well as in other standard implementations, but very simple only two transistors per function is required in the GDI design technique. In this paper, most of the considered circuits were based on the F1 and F2 functions. The reasons for this are as follows.

1) Both F1 and F2 are complete logic families (allows realization of any possible two-input logic function).

2) F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased.

3) When N input is driven at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to out are directly polarized and there is a short between N and P, resulting in static power dissipation.

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Out</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>‘0’</td>
<td>B</td>
<td>A</td>
<td>$\bar{A}B$</td>
<td>F1</td>
</tr>
<tr>
<td>B</td>
<td>‘1’</td>
<td>A</td>
<td>$A + B$</td>
<td>F2</td>
</tr>
<tr>
<td>‘1’</td>
<td>B</td>
<td>A</td>
<td>$A + B$</td>
<td>OR</td>
</tr>
<tr>
<td>B</td>
<td>‘0’</td>
<td>A</td>
<td>$AB$</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>$\bar{A}B + AC$</td>
<td>MUX</td>
</tr>
<tr>
<td>‘0’</td>
<td>‘1’</td>
<td>A</td>
<td>$\bar{A}$</td>
<td>NOT</td>
</tr>
</tbody>
</table>

The GDI cell structure is different from the existing CMOS techniques and has some important features, which allow improvements in design complexity level, transistor count, and power dissipation.

IV. CMOS BASIC LOGIC GATES

1. OR Gate Using CMOS Technique

The OR gate Cell is designed for a minimal number of transistors in CMOS logic technique as shown in Fig.2.

Where A and B are Inputs, Vdd is 1.8V output is measured across ‘Out’. A CMOS OR gate circuit uses Six MOSFETs. In the OR gate uses two series-connected sourcing transistors connected to Vdd and two parallel-connected sinking transistors connected to Ground and one inverter in series to sinking transistor.

2. AND Gate Using CMOS Technique

In the Fig. 3. NAND gate circuit is connected in series with CMOS inverter. Where Notice how transistors $Q_1$ and $Q_3$ resemble the series-connected complementary pair from the inverter circuit.

Both are controlled by the same input signal (input A), the upper transistor turning off and the lower transistor turning on when the input is “high” (1), and vice versa. Notice also how transistors $Q_2$ and $Q_4$ are similarly controlled by the same input signal (input B), and how they will also exhibit the same on/off behavior for the same input logic levels.
Fig. 4. X-OR Gate in CMOS logic.

The upper transistors of both pairs ($Q_1$ and $Q_2$) have their source and drain terminals paralleled, while the lower transistors ($Q_3$ and $Q_4$) are series-connected. What this means is that the output will go “high” (1) if either top transistor saturates, and will go “low” (0) only if both lower transistors saturate.

The following sequence of illustrations shows the behavior of this NAND gate for all four possibilities of input logic levels (00, 01, 10, and 11). Fig. 4. Shows CMOS implementation of X-OR gate.

V. GDI LOGIC GATES

Wishing to cover a wide range of possible circuits, design methods, and properties comparisons, several digital combinatorial circuits were implemented using CMOS and GDI methods design techniques, and technology processes. The AND, OR, and XOR Cells are implemented using GDI technique as shown in Fig. 5. Fig. 6. And Fig. 7. contains AND, OR, and XOR cells using GDI respectively. It must be noticed that use of the full GDI library is not possible in a regular p-well CMOS process. As a result, only function F1 (as mention in Table I) and its expansions could be implemented. The Fig. 5. to Fig. 7. Shows implementation of GDI basic functions for a regular p-well process.

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VI. GDI COMPARISONS WITH OTHER LOGIC STYLES

Circuits were designed at the transistor level in a 0.18µm P-well CMOS process technology (Vdd = 1.8V). The circuits were simulated using Microwind 3 at 1.8V, 40 MHz with load capacitance of 100 fF. In our simulations, the well capacitance and other parasitic parameters were not taken into account. Each set includes a logic cell implemented in two different techniques: GDI and CMOS. Cells were designed for a minimal number of transistors in each technique as shown in Table II. Most circuits where implemented with ratio of three to achieve the best power-delay performance same transitions of logic values were supplied to the inputs of the test circuits in each technique.

| Table II: TRANSISTOR COUNT FOR DIFFERENT TECHNIQUES |
|----------------|-----|------|
|               | GDI | CMOS |
| AND           | 4   | 6    |
| OR            | 6   | 6    |
| X-OR          | 10  | 12   |

For each technique, average power, maximal delay, and number of transistors were measured. Among all the design techniques, GDI proves to have the minimal number of transistors.

Each GDI gate was implemented using only two transistors. Comparison of simulation result is ass shown in Table III.

| Table III: SIMULATION RESULT OF GDI AND CMOS LOGIC GATES |
|----------------|-----|------|------|
| SPECIFICATION  | CMOS   | GDI    | [1]  |
| Technology     | 0.18µm | 0.18µm | 0.35µm|
| Vdd            | 1.8V   | 1.8V   | 3.3V  |
| Power of OR    | 26 pW  | 25.4pW | 26.3pW|
| Gate           | 200nm  | 200nm  | 350nm |

VII. CONCLUSION

A novel GDI technique for low-power design was presented. Among the presented design techniques, GDI proves to have the finest performance values and lowest transistor count. Most of the circuits were implemented in regular p-well a CMOS process, GDI cell library having limited functions. Still, even in limited-library-based GDI circuits, significant improvements of performance are observed.

REFERENCES


